IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) ~~An integrated~~ A display unit ~~with~~ comprising:

[[-]] a display ~~with a plurality of~~ including display elements ~~(Dx)~~ which are combined into ~~a plurality of~~ groups of display elements,

[[-]] a circuit arrangement for controlling the display ~~with a plurality of~~, the circuit arrangement including switches and inverters which are connected in series to form a series arrangement, ~~(Sw1, Sw2, ...) which can be closed with a first clock signal and opened with a second clock signal, and with a plurality of inverters (In1, In2, ...), wherein the switches and inverters are connected in series in mutual alternation, such that~~

[[-]] each group of the groups of display elements ~~(Dx)~~ is

connected to an output of an inverter ~~(In1, In2, ...) each~~, and ~~with~~

[[-]] at least one clock bus line ~~(Φ1, Φ2) via which the~~ to supply a first clock signal and ~~the~~ a second clock ~~signal are supplied in alternation to the first, third, fifth, etc. switch (Sw1, Sw3, Sw5, ...) of the series arrangement, and the second and the first clock signal are supplied in alternation to the second, fourth, sixth, etc. switch (Sw2, Sw4, Sw6, ...)~~, wherein a first set of switches is closed with the first clock signal when a second set of switches is opened with the second clock signal so that after ~~the~~ consecutive application of a third clock signal to ~~the~~ an input of the series arrangement, ~~consecutively at a time~~ at least one of the groups of display elements ~~(Dx)~~ is activated.

2.(Currently Amended) ~~An~~ The integrated display unit as claimed in claim 1, ~~with~~ comprising a carrier on which the display elements ~~(Dx)~~ are arranged in ~~the form of~~ a display field, wherein the at least one clock bus line ~~(Φ1, Φ2)~~ extends along ~~the~~ an edge of the display field.

3. (Currently Amended) ~~An~~ The integrated display unit as claimed in claim 1, wherein the groups of display elements ~~(Dx)~~ are each formed by a row or a column of a matrix display.

4. (Currently Amended) ~~An~~ The integrated display unit as claimed in claim 1, wherein each switch of the switches ~~(Sw1, Sw2, . . .) are each~~ is formed by ~~an~~ a first n-transistor, and each inverter of the inverters ~~(In1, In2, . . .) are each~~ is formed by a parallel arrangement of a p-transistor and ~~an~~ a second n-transistor.

5. (Currently Amended) ~~An~~ The integrated display unit as claimed in claim 1, wherein the groups of display elements ~~(Dx) in the non-interlaced control of said groups~~ are connected to respective outputs of the ~~second, fourth, sixth, etc. inverter (In2, In4, In6, . . .)~~ inverters of the series arrangement.

6. (Currently Amended) ~~An~~ The integrated display unit as claimed in claim 5, wherein the groups of display elements ~~(Dx) are~~ include ~~the~~ sampled rows or sampled columns of a matrix display.

7. (Currently Amended) ~~An~~ The integrated display unit as claimed in claim 1, wherein the groups of display elements ~~(Dx) for the interlaced control of said groups can~~ are each ~~be~~ connected via a converter ~~(Um1, Um2, ...)~~ to a ~~fifth or sixth~~ further clock bus line ~~(B1, A2)~~ for ~~the~~ a half-image switch-over, and ~~the~~ converters ~~(Um1, Um2, ...) can each be~~ are switched over by ~~means of~~ a signal applied to ~~the~~ an input and/or ~~the~~ an output of ~~the~~ an associated inverter ~~(In1, In2, ...)~~.

8. (Currently Amended) ~~An~~ The integrated display unit as claimed in claim 7, wherein the converters ~~(Um1, Um2, ...)~~ are formed by two on/off switches each comprising a p- and an n-transistor.

9. (Currently Amended) ~~An~~ The integrated display unit as claimed in claim 7, wherein the groups of display elements ~~(Dx)~~ are ~~the~~ sampled rows and/or ~~the~~ sampled scanning columns and/or ~~the~~ data rows and/or ~~the~~ data columns of a matrix display.

10.(New) The display unit of claim 1, wherein the display elements are arranged in N rows and M columns, and wherein a number of external connections for controlling the display unit is N+M.

11.(New) The display unit of claim 1, wherein the display elements are arranged in N rows, and wherein a number of external connections for controlling the display unit is 5 or 7.

12.(New) A display unit comprising:

display elements;

series arrangements between the display elements, wherein each of the series arrangements includes a first switch connectable to a first inverter and a second switch connectable to a second inverter;

a first bus for a first clock for controlling the first switch;

a second bus for a second clock for controlling the second switch;

wherein the first switch and the second switch are alternately

controlled by the first clock and the second clock, respectively, so that when the first switch is opened then the second switch is closed; and

a third bus for a third clock for application to an input of one of the series arrangements so that groups of the display elements are consecutively activated.

13. (New) The display unit of claim 12, wherein the display elements are arranged in N rows and M columns, and wherein a number of external connections for controlling the display unit is N+M.

14. (New) The display unit of claim 12, wherein the display elements are arranged in N rows, and wherein a number of external connections for controlling the display unit is 5 or 7.

15. (New) The display unit of claim 12, wherein at least one of the first bus and the second bus is arranged along an edge of the display unit.

16. (New) A display unit comprising:

a first inverter;

a first switch connected to an input of the first inverter;

a second switch connected between an output of the first inverter and an input of a second inverter;

a first display element connectable through a third switch to the input of the first inverter and connectable through a fourth switch to the output of the first inverter;

a second display connectable through a fifth switch to the input of the second inverter and connectable through a sixth switch to an output of the second inverter; and

clock buses for supplying a first clock to control the first switch and a second clock to control the second switch, and a third clock to one terminal of the first switch, wherein the first switch and the second switch are alternately controlled by the first clock and the second clock, respectively, so that when the first switch is opened then the second switch is closed in order to consecutively activate the first display element and the second display element.

17. (New) The display unit of claim 16, further comprising

additional display elements that are arranged in N rows and M columns, and wherein a number of external connections for controlling the display unit is N+M.

18.(New) The display unit of claim 16, further comprising additional display elements that are arranged in N rows, and wherein a number of external connections for controlling the display unit is 5 or 7.

19.(New) The display unit of claim 16, wherein at least one of the clock buses is arranged along an edge of the display unit.